

# FDN336P

## Single P-Channel 2.5V Specified PowerTrench® MOSFET

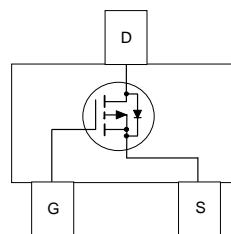
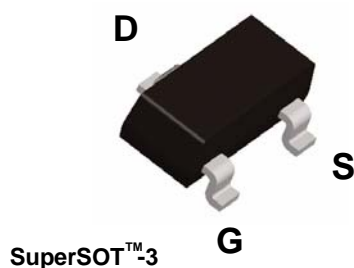
### General Description

This P-Channel 2.5V specified MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

These devices are well suited for portable electronics applications: load switching and power management, battery charging circuits and DC/DC conversion.

### Features

- -1.3 A, -20 V.  $R_{DS(ON)} = 0.20 \Omega @ V_{GS} = -4.5 V$   
 $R_{DS(ON)} = 0.27 \Omega @ V_{GS} = -2.5 V$
- Low gate charge (3.6 nC typical)
- High performance trench technology for extremely low  $R_{DS(ON)}$
- SuperSOT™ -3 provides low  $R_{DS(ON)}$  and 30% higher power handling capability than SOT23 in the same footprint



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage	-20	V
V <sub>GSS</sub>	Gate-Source Voltage	±8	V
I <sub>D</sub>	Drain Current – Continuous (Note 1a)	-1.3	A
	– Pulsed	-10	
P <sub>D</sub>	Maximum Power Dissipation (Note 1a) (Note 1b)	0.5	W
		0.46	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	75	°C/W

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
336	FDN336P	7"	8mm	3000 units

## Electrical Characteristics ( $T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = -250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$		-16		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
		$T_J = 55\text{ }^\circ\text{C}$			-10	$\mu\text{A}$
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
<b>ON CHARACTERISTICS (Note 2)</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.4	-0.9	-1.5	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = -250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$		3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -4.5\text{ V}, I_D = -1.3\text{ A}$		0.122	0.2	$\Omega$
		$T_J = 125\text{ }^\circ\text{C}$		0.18	0.32	
		$V_{GS} = -2.5\text{ V}, I_D = -1.1\text{ A}$		0.19	0.27	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-5			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -4.5\text{ V}, I_D = -2\text{ A}$		4		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		330		pF
$C_{oss}$	Output Capacitance			80		pF
$C_{rss}$	Reverse Transfer Capacitance			35		pF
<b>SWITCHING CHARACTERISTICS (Note 2)</b>						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = -5\text{ V}, I_D = -0.5\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$		7	15	ns
$t_r$	Turn - On Rise Time			12	22	ns
$t_{D(off)}$	Turn - Off Delay Time			16	26	ns
$t_f$	Turn - Off Fall Time			5	12	ns
$Q_g$	Total Gate Charge	$V_{DS} = -10\text{ V}, I_D = -2\text{ A},$ $V_{GS} = -4.5\text{ V}$		3.6	5	nC
$Q_{gs}$	Gate-Source Charge			0.8		nC
$Q_{gd}$	Gate-Drain Charge			0.7		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				-0.42	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -0.42\text{ A}$ (Note)		-0.7	-1.2	V

Note:

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $250\text{ }^\circ\text{C/W}$  when mounted on  
a  $0.02\text{ in}^2$  pad of 2oz Cu.



b.  $270\text{ }^\circ\text{C/W}$  when mounted on  
a  $0.001\text{ in}^2$  pad of 2oz Cu.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## Typical Electrical Characteristics

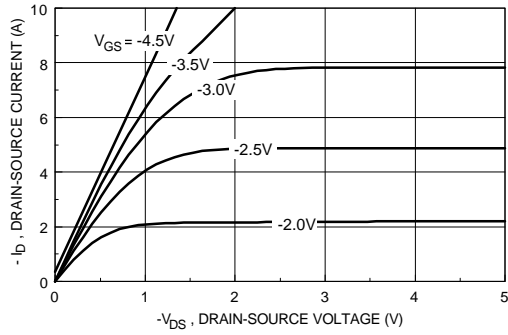


Figure 1. On-Region Characteristics.

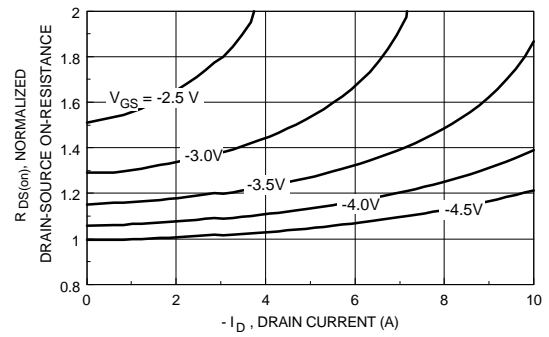


Figure 2. On-Resistance Variation with Drain Current and Gate

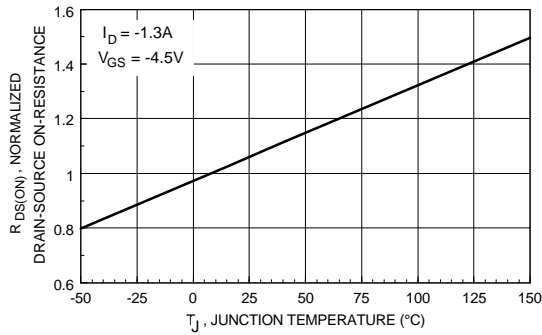


Figure 3. On-Resistance Variation with Temperature.

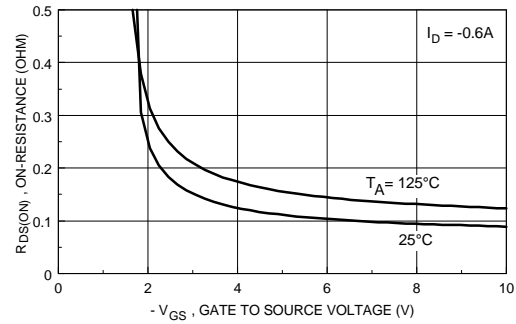


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

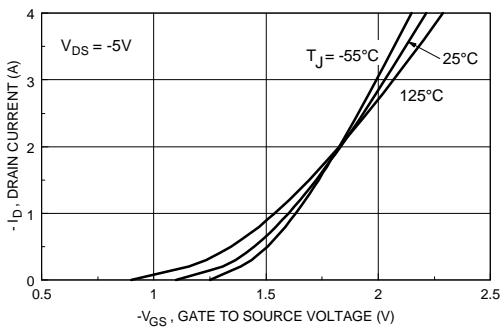


Figure 5. Transfer Characteristics.

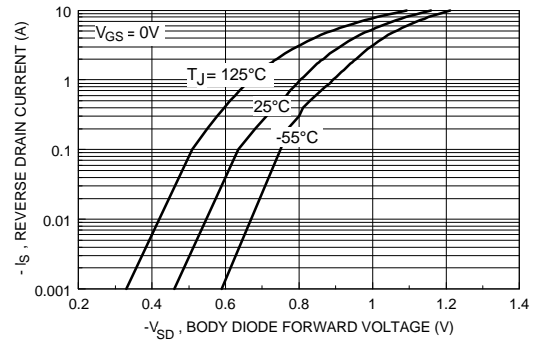


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Electrical Characteristics (continued)

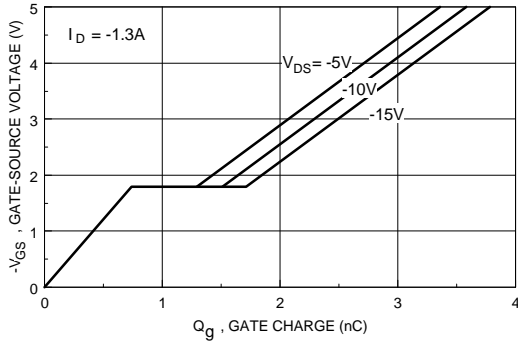


Figure 7. Gate Charge Characteristics.

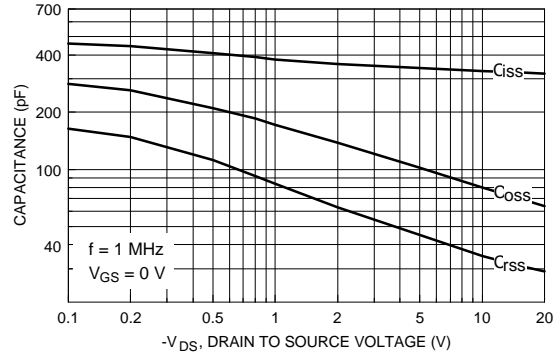


Figure 8. Capacitance Characteristics.

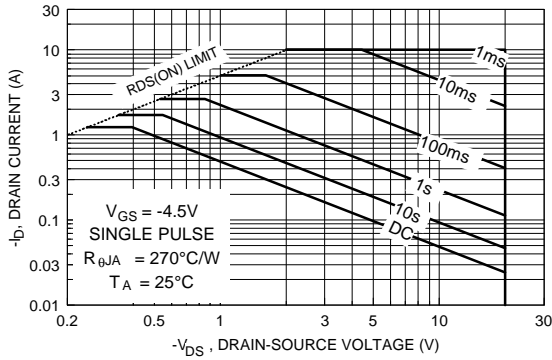


Figure 9. Maximum Safe Operating Area.

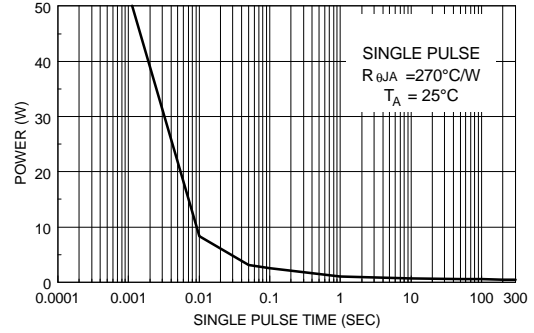


Figure 10. Single Pulse Maximum Power Dissipation.

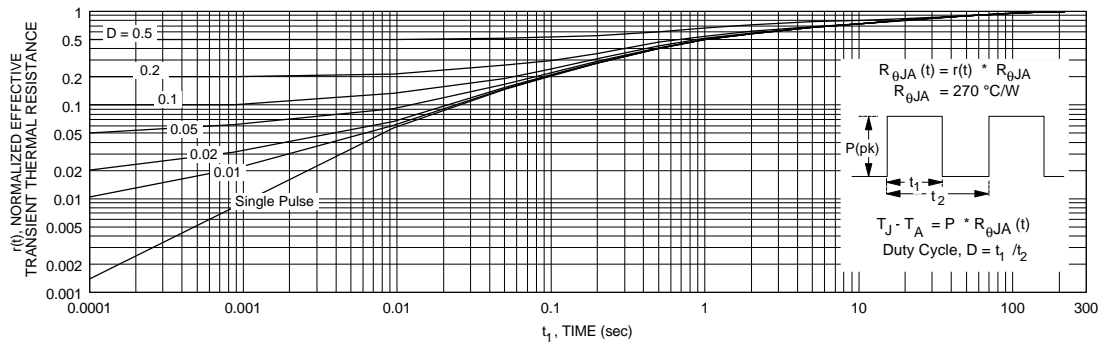


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.  
Transient thermal response will change depending on the circuit board design.

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